WHAT IS CLAIMED IS:

1. An image processing architecture for an image input apparatus, comprising:

a ping-pong buffer having multiple rows for storing image data;

an image data storage media for storing correction data used to correct the input image, and the said storage media is used to store the corrected image according to the said correction data; and

a first cache memory for storing the correction data read from the image storage media and for providing the correction data to a digital controller to correct the said input image according to the correction data.

2. The image processing architecture as defined in claim 1, further including a second cache memory which is used as a work space for line-difference compensation data arrangement of the said input image.

3. A method of processing an scanned image, comprising:

a. storing image to one of the rows of the said ping-pong buffer;

b. reading correction data required for image correction from the cache memory;

c. correcting the said input image according to the correction data, and storing the succeeding input image to another rows, the said succeeding input image is received from the input signal processor; and

d. correcting the said input image sequentially while the previous image data is corrected.

4. The method of processing a scanned image as defined in claim 3, further comprising:

storing corrected image;

reading RGB data of the corrected image;

performing line-difference compensation; and

arranging image data in pixel rate order.